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WORKED EXAMPLES

D. A. JACOBS, B.Sc., C.ENG., M.I.E.E.

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PART 1—Electrical and Electronic Principles III (BTEC)

Q1 For the circuit shown in Figure 1 calculate the resistance between A and D.

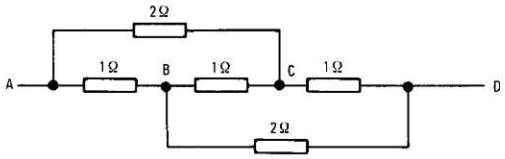
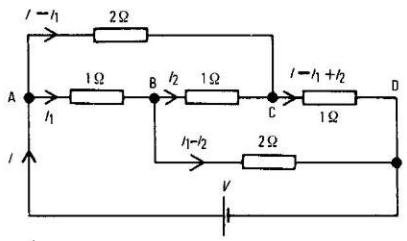


Figure 1

A1

The arrangement of the circuit is such that it is not possible to solve the network by straight-forward series-parallel calculations. The circuit could be solved by the use of delta-star transformation, but this is beyond the scope of Level III work. The circuit should be redrawn and connected to a supply voltage, after which the circuit current can be obtained. Using the circuit current, the resistance can be calculated.



By Kirchhoff's Law,

Loop ACBA

$$2(I - I_1) - I_2 - I_1 = 0.$$

$$\therefore \quad 2I - 2I_1 - I_2 - I_1 = 0.$$

$$\therefore \quad 2I - 3I_1 - I_2 = 0. \tag{1}$$

Loop BCDB

$$I_2 + (I - I_1 + I_2) - 2(I_1 - I_2) = 0.$$

$$\therefore \quad I_2 + I - I_1 + I_2 - 2I_1 + 2I_2 = 0.$$

$$\therefore \quad I - 3I_1 + 4I_2 = 0. \tag{2}$$

Loop ABCDA

$$I_1 + I_2 + (I - I_1 + I_2) - V = 0.$$

$$\therefore \quad I_1 + I_2 + I - I_1 + I_2 - V = 0.$$

$$\therefore \quad I + 2I_2 = V. \tag{3}$$

Subtracting equation (2) from equation (1) to eliminate I_1,

$$2I - 3I_1 - I_2 = 0. \tag{1}$$

$$\underline{I - 3I_1 + 4I_2 = 0.} \tag{2}$$

$$I - 5I_2 = 0. \tag{4}$$

Eliminating I_2,

$$5 \times (3) \qquad 5I + 10I_2 = 5V. \tag{5}$$

$$2 \times (4) \qquad 2I - 10I_2 = 0. \tag{6}$$

Adding equation (5) and equation (6),

$$7I = 5V.$$

$$\therefore \quad I = \tfrac{5}{7}V.$$

The resistance across the network,

$$R_{AD} = \frac{V}{I} = \frac{V}{\frac{5}{7}V} = \tfrac{7}{5}\,\Omega = \underline{1{\cdot}4\,\Omega.}$$

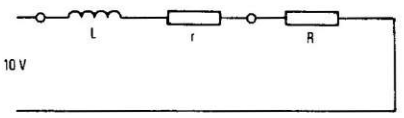
Q2 *An inductor L of resistance 0·5 Ω is connected in series with a resistor R. When the circuit is connected to a supply of 10 V, 200 Hz, the current is 1 A. When the circuit is connected to 10 V, 400 Hz, the current is 0·8 A.*

(*a*) *Calculate the*

(*i*) *inductance of the inductor,*
(*ii*) *value of the resistor R,*
(*iii*) *impedance of the inductor at 200 Hz,*
(*iv*) *circuit current when the supply is 10 V, 1000 Hz,*
(*v*) *maximum current if the voltage is constant at 10 V but the frequency variable.*

(*b*) *Sketch a graph of the variation of the circuit current with respect to frequency.*

A2



The solution is not readily obtainable by a direct method. The value of L can be obtained by setting up a pair of simultaneous equations after which the circuit resistance can be eliminated.

(*a*) (*i*) For the series circuit,

$$V_Z^2 = V_{R+r}^2 + V_L^2.$$

$$\therefore \quad V_Z^2 = I^2(R+r)^2 + I^2X_L^2.$$

$$\therefore \quad \left(\frac{V_Z}{I}\right)^2 = (R+r)^2 + (\omega L)^2.$$

At 200 Hz, $$\left(\frac{10}{1}\right)^2 = (R+r)^2 + (2\pi \times 200L)^2.$$

$$\therefore \quad 100 = (R+r)^2 + (400\pi L)^2. \tag{1}$$

At 400 Hz, $$\left(\frac{10}{0{\cdot}8}\right)^2 = (R+r)^2 + (2\pi \times 400L)^2.$$

$$\therefore \quad 156{\cdot}25 = (R+r)^2 + (800\pi L)^2. \tag{2}$$

Subtracting equation (1) from equation (2),

$$56{\cdot}25 = (800\pi L)^2 - (400\pi L)^2.$$

$$\therefore \quad 56{\cdot}25 = (100\pi L)^2(8^2 - 4^2).$$

$$\therefore \quad 56{\cdot}25 = (100\pi L)^2(48).$$

$$\therefore \quad L^2 = \frac{56{\cdot}25}{48(100\pi)^2}.$$

$$\therefore \quad L = \frac{1}{100\pi}\sqrt{\left(\frac{56{\cdot}25}{48}\right)}\,\text{H} = \underline{3{\cdot}446\,\text{mH.}}$$

(*ii*) $Z = V/I$; therefore at 200 Hz, $Z = 10/1 = 10\,\Omega$.

Also, $$Z^2 = (R+r)^2 + (\omega L)^2.$$

$$\therefore \quad (R+r)^2 = Z^2 - (\omega L)^2,$$

$$= 10^2 - (2\pi \times 200 \times 3{\cdot}446 \times 10^{-3})^2,$$

$$= 100 - 18{\cdot}752 = 81{\cdot}248.$$

$$\therefore \quad R + r = \sqrt{81{\cdot}248} = 9{\cdot}014\,\Omega.$$

$$\therefore \quad R = 9{\cdot}014 - 0{\cdot}5\,\Omega = \underline{8{\cdot}514\,\Omega.}$$

(*iii*) The reactance of the inductor,

$$X_L = 2\pi f L.$$

At 200 Hz, $X_L = 2\pi \times 200 \times 3{\cdot}446 \times 10^{-3}\,\Omega = 4{\cdot}33\,\Omega$

$$\therefore \quad Z_L = \sqrt{(r^2 + X_L^2)} = \sqrt{(0{\cdot}5^2 + 4{\cdot}33^2)} = \underline{4{\cdot}359\,\Omega.}$$

(*iv*) At 1000 Hz, $X_L = 2\pi \times 1000 \times 3{\cdot}446 \times 10^{-3}\,\Omega = 21{\cdot}652\,\Omega.$

Now, $$Z = \sqrt{\{(R+r)^2 + X_L^2\}}$$

At 1000 Hz, $$Z = \sqrt{\{9{\cdot}014^2 + 21{\cdot}652^2\}}\,\Omega = 23{\cdot}45\,\Omega.$$

At 1000 Hz, the circuit current will be

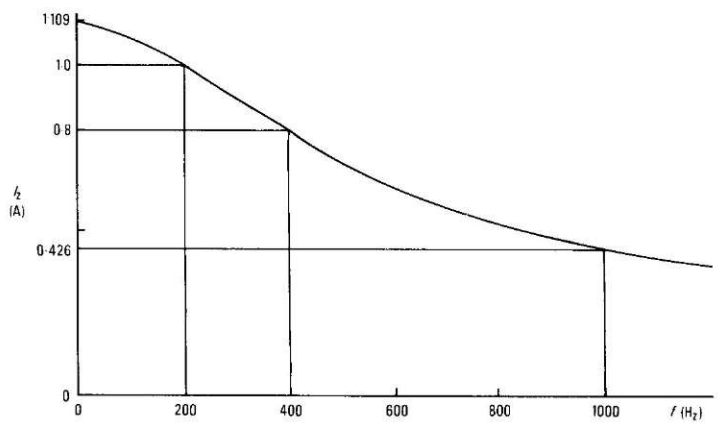
$$I = \frac{V}{Z} = \frac{10}{23{\cdot}45}\,\text{A} = \underline{0{\cdot}426\,\text{A.}}$$

(*v*)

When the frequency is 0 Hz (that is, a DC supply), the inductive reactance will be zero and maximum current will flow in the circuit, because the only opposition to current flow is the circuit resistance.

$$\therefore \quad I_{max} = \frac{V}{R+r} = \frac{10}{9{\cdot}014} = 1{\cdot}109\,\text{A.}$$

(*b*)



Q3 *The circuit shown in Figure 2 is that of a parallel low-Q network where the inductive element has a resistance of 60 Ω. The supply connected to the circuit is 200 V, 50 Hz.*

(*a*) *Show that the circuit is not operating at the frequency of resonance.*
(*b*) *Calculate the current in the inductive arm and that in the capacitive arm.*
(*c*) *Sketch the phasor diagram for the circuit.*
(*d*) *Calculate the supply current, the circuit impedance and the circuit power dissipation.*

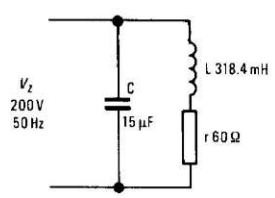


Figure 2

A3

Since the circuit is stated to be low Q, the approximate formula for the frequency of resonance is not used.

(a) For a parallel circuit, the frequency of resonance,

$$f = \frac{1}{2\pi}\sqrt{\left\{\frac{1}{LC} - \frac{r^2}{L^2}\right\}},$$

$$= \frac{1}{2\pi}\sqrt{\left\{\frac{1}{318{\cdot}4 \times 10^{-3} \times 15 \times 10^{-6}} - \left(\frac{60}{318{\cdot}4 \times 10^{-3}}\right)^2\right\}} \text{ Hz},$$

$$= \frac{1}{2\pi}\sqrt{\{0{\cdot}2094 \times 10^6 - 0{\cdot}0355 \times 10^6\}} = 66{\cdot}37 \text{ Hz}.$$

Since the supply is at 50 Hz, the circuit is not operating at the frequency of resonance.

(b) The reactance of the inductor,

$$X_L = 2\pi f L = 2\pi \times 50 \times 318{\cdot}4 \times 10^{-3}\,\Omega = 100\,\Omega.$$

The impedance of the inductance/resistance combination,

$$Z_{Lr} = \sqrt{(r^2 + X_L^2)} = \sqrt{(60^2 + 100^2)} = 116{\cdot}62\,\Omega.$$

Thus, the current in the inductive arm,

$$I_{Lr} = \frac{V_Z}{Z_{Lr}} = \frac{200}{116{\cdot}62} = \underline{1{\cdot}715 \text{ A}.}$$

The reactance of the capacitor,

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 50 \times 15 \times 10^{-6}}\,\Omega = 212{\cdot}2\,\Omega.$$

The current in the capacitive arm,

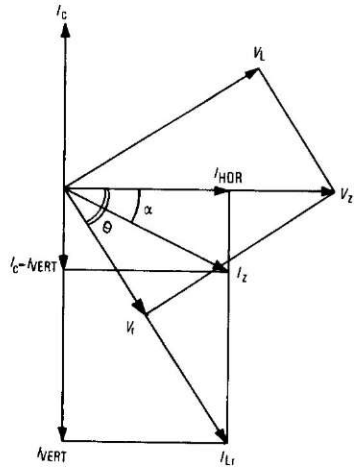
$$I_C = \frac{V_Z}{X_C} = \frac{200}{212{\cdot}2} \text{ A} = \underline{0{\cdot}9425 \text{ A}.}$$

In order to sketch the phasor diagram, the phase of the inductive current is needed. The presence of the resistance in the inductive arm has the effect of moving the phase angle away from 90 degrees.

(c) The phase angle,

$$\theta = \tan^{-1}\left(\frac{X_L}{r}\right) = \tan^{-1}\left(\frac{100}{60}\right) = 59°.$$

In the phasor diagram, the inductive current will lag the supply voltage by 59°.



In the phasor diagram, the inductive current lags the supply voltage by angle θ. Since this current flows through r the potential difference across r must also lag the supply voltage by angle θ. The phasor sum of V_r and V_L must add up to the supply voltage and this is also shown. Note that V_L leads I_{Lr} by 90°. To find the supply current, the inductive current must be used to find the horizontal and vertical components, after which the vertical component is subtracted from I_C. The solution for I_Z then follows by the use of Pythagoras' Theorem.

(*d*)

$$I_{HOR} = I_{Lr} \cos\theta = 1{\cdot}715 \cos(-59°) = 0{\cdot}8833 \text{ A}.$$

$$I_{VERT} = I_{Lr} \sin\theta = 1{\cdot}715 \sin(-59°) = -1{\cdot}47 \text{ A}.$$

$$I_C + I_{VERT} = 0{\cdot}9425 + (-1{\cdot}47) \text{ A} = -0{\cdot}5275 \text{ A}.$$

Thus, the supply current,

$$I_Z = \sqrt{\{I_{HOR}^2 + (I_C + I_{VERT})^2\}} = \sqrt{\{0{\cdot}8833^2 + (-0{\cdot}5275)^2\}} \text{ A} = \underline{1{\cdot}0288 \text{ A}}.$$

The supply current lags the supply voltage by the angle α shown in the phasar diagram and it can be calculated as follows.

$$\alpha = \tan^{-1}\frac{(I_C + I_{VERT})}{I_{HOR}} = \tan^{-1}\left(\frac{-0{\cdot}5275}{0{\cdot}8833}\right) = -30{\cdot}845°.$$

The circuit impedance is given by,

$$Z = \frac{V_Z}{I_Z} = \frac{200}{1{\cdot}0288}\ \Omega = \underline{194{\cdot}4\ \Omega}.$$

The only power dissipated in the circuit is in the resistance of the inductor,

$$P = I_{Lr}^2 r = 1{\cdot}715^2 \times 60 \text{ W} = \underline{176{\cdot}47 \text{ W}}.$$

The circuit power can also be found by the use of the formula $VI\cos\alpha$, but in the case where only the power dissipation is required, it is much quicker to calculate I_{Lr} and then use it directly. However, calculating $VI\cos\alpha$,

$$P = V_Z I_Z \cos\alpha = 200 \times 1{\cdot}0288 \cos 30{\cdot}845° \text{ W} = 176{\cdot}66 \text{ W}.$$

This result produces a slightly different value but it occurs because of the rounding off of the values throughout the calculation.

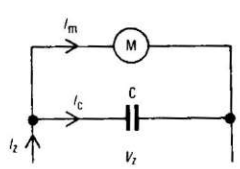
Q4 *A motor which operates from a supply of 240 V, 50 Hz takes a current of 15 A, at a lagging power factor of 0·48. Operating regulations require that the power factor is increased to 0·92.*

(*a*) *Draw the circuit showing the motor and any additional component required to obtain the change of power factor.*
(*b*) *Draw a phasor diagram which shows the voltage and currents before and after correction.*
(*c*) *Calculate the supply current after the power factor has been increased to 0·92.*
(*d*) *Find the value of any additional component shown in* (*a*).

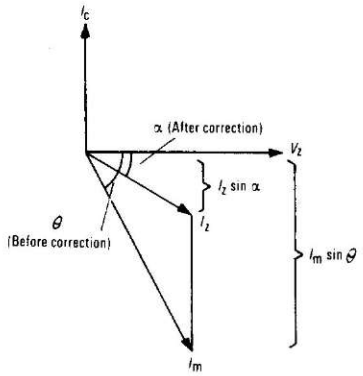
A4

The motor has a lagging power factor which implies that it is inductive. In order to increase the power factor, capacitance is introduced to offset part of the inductive reactance. The capacitor is connected in parallel with the motor (if the capacitor were placed in series with the motor, the motor potential difference would no longer be 240 V).

(*a*)



(*b*)



The real power in the circuit is the same before and after power factor correction, so the value of I_Z can be found as follows:

$$P = VI \cos \phi, \qquad \text{where} \qquad \cos \phi \text{ is the power factor.}$$

$$\therefore \qquad P = V_Z I_m \cos \theta = V_Z I_Z \cos \alpha.$$

$$\therefore \qquad I_m \cos \theta = I_Z \cos \alpha.$$

$$\therefore \qquad I_Z = \frac{I_m \cos \theta}{\cos \alpha}$$

(*c*)
$$I_Z = \frac{I_m \cos \theta}{\cos \alpha} = \frac{15 \times 0{\cdot}48}{0{\cdot}92} = \underline{7{\cdot}826 \text{ A.}}$$

The capacitor must have such a value to reduce the vertical component of I_m to the vertical component of I_Z. This means that the magnitude of I_C is given by

$$|I_C| = I_m \sin \theta - I_Z \sin \alpha.$$

(*d*)
$$\theta = \cos^{-1} 0{\cdot}48 = 61{\cdot}3°$$

$$\alpha = \cos^{-1} 0{\cdot}92 = 23{\cdot}074°$$

$$\therefore \qquad |I_C| = 15 \sin 61{\cdot}3° - 7{\cdot}826 \sin 23{\cdot}074° \text{ A} = 13{\cdot}159 - 3{\cdot}067 \text{ A} = 10{\cdot}092 \text{ A.}$$

The reactance of the capacitor is given by

$$X_C = \frac{V_Z}{I_C} = \frac{240}{10{\cdot}092} = 23{\cdot}78\ \Omega.$$

Also,

$$X_C = \frac{1}{2\pi f C}.$$

$$\therefore \qquad C = \frac{1}{2\pi f X_C} = \frac{1}{2\pi \times 50 \times 23{\cdot}78} \text{ F} = \underline{133{\cdot}86\ \mu\text{F.}}$$

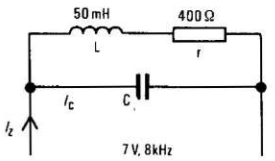
Q5 *A coil of inductance 50 mH and resistance 400 Ω is connected in parallel with a capacitor. The complete circuit is then connected to a supply of 7 V, 8 kHz.*

(*a*) *Calculate the value of capacitor which will reduce the supply current to its minimum value.*

(*b*) *Calculate the* Q *value for the circuit when the circuit is tuned to the frequency of resonance.*

(*c*) *Draw a sketch of the variation of current with frequency for the circuit.*

A5



For the parallel circuit, the current taken from the supply will be a minimum at the frequency of resonance. If the Q value were known to be high (at least 10) the approximate formula could be used but in this case, since there is some doubt (suggested by the high value of r) the accurate formula must be used.

(*a*) The frequency of resonance is given by

$$f_0 = \frac{1}{2\pi}\sqrt{\left(\frac{1}{LC} - \frac{r^2}{L^2}\right)}.$$

$$\therefore \quad (2\pi f)^2 = \frac{1}{LC} - \frac{r^2}{L^2}.$$

$$\therefore \quad \frac{1}{LC} = (2\pi f)^2 + \frac{r^2}{L^2}.$$

$$\therefore \quad \frac{1}{C} = \left\{(2\pi f)^2 + \frac{r^2}{L^2}\right\}L,$$

$$= \left\{(2\pi \times 8000)^2 + \left(\frac{400}{50 \times 10^{-3}}\right)^2\right\}50 \times 10^{-3},$$

$$= (2{\cdot}5266 \times 10^9 + 64 \times 10^6)50 \times 10^{-3},$$

$$= 129{\cdot}53 \times 10^6\ \mathrm{F}^{-1}.$$

$$\therefore \quad C = 7{\cdot}72 \times 10^{-9}\ \mathrm{F} = \underline{7{\cdot}72\ \mathrm{nF}}.$$

The Q value can be found from

$$Q = \frac{I_C}{I_Z},$$

where

$$I_Z = \frac{V_Z}{Z_D} \quad \text{and} \quad I_C = \frac{V_Z}{X_C}.$$

$$\therefore \quad Q = \frac{I_C}{I_Z} = \frac{V_Z/X_C}{V_Z/Z_D} = \frac{Z_D}{X_C} = \frac{Z_D}{1/\omega C} = Z_D\omega C.$$

(*b*) At resonance,

$$Z_D = \frac{L}{Cr} = \frac{50 \times 10^{-3}}{7{\cdot}72 \times 10^{-9} \times 400}\ \Omega = 16\,192\ \Omega.$$

$$\therefore \quad Q = 16\,192 \times 2\pi \times 8000 \times 7{\cdot}72 \times 10^{-9} = \underline{6{\cdot}283}.$$

(*c*) The minimum current

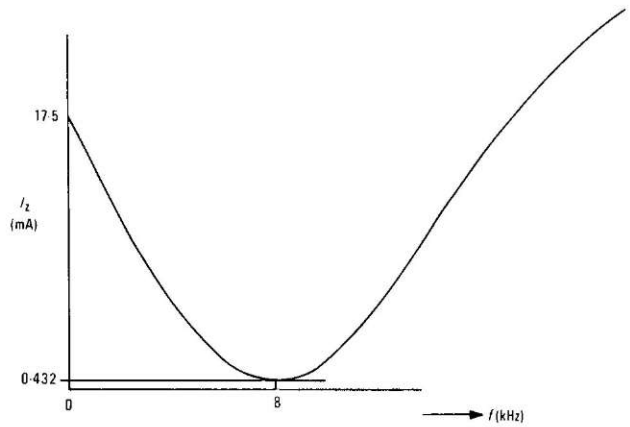
$$I_{min} = \frac{V_Z}{Z_D} = \frac{7}{16\,192}\ \mathrm{A} = 0{\cdot}432\ \mathrm{mA}.$$

When $f = 0$ Hz, no current flows through the capacitor but the inductive arm, whose reactance is zero, passes a current limited only by r.

At $f = 0$ Hz,

$$I_r = \frac{V_Z}{r} = \frac{7}{400}\text{ A} = 17{\cdot}5\text{ mA}.$$

The sketch of the variation of current with frequency is as follows.

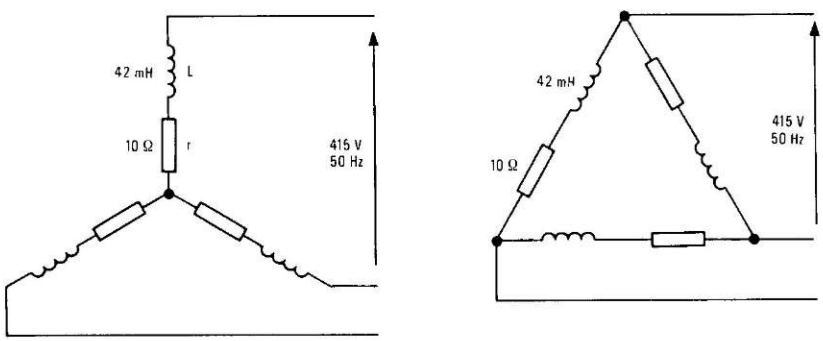


Q6 *Three identical coils of resistance 10 Ω and inductance 42 mH are connected to a three-phase supply of 415 V, 50 Hz.*

Calculate the circuit power factor and determine the power dissipation when the coils are connected in

(*a*) *star, and*
(*b*) *delta.*

A6



The reactance of each coil,

$$X_L = 2\pi f L = 2\pi \times 50 \times 42 \times 10^{-3}\,\Omega = 13{\cdot}195\,\Omega.$$

Therefore, the impedance of each resistance/inductance combination,

$$Z_L = \sqrt{(r^2 + X_L^2)} = \sqrt{(10^2 + 13{\cdot}195^2)}\,\Omega = 16{\cdot}56\,\Omega.$$

$$\text{Power factor} = \cos\theta = \frac{r}{Z_L} = \frac{10}{16{\cdot}56} = \underline{0{\cdot}604.}$$

(*a*) By inspection of the circuit, the phase voltage in star can be seen to be less than the line voltage

$$\therefore \quad V_{PHASE} = \frac{V_{LINE}}{\sqrt{3}} = \frac{415}{\sqrt{3}} = 239{\cdot}6\text{ volts}.$$

$$I_{PHASE} = \frac{V_{PHASE}}{Z_L} = \frac{239{\cdot}6}{16{\cdot}56} = 14{\cdot}47\text{ A}.$$

For the three loads, the power dissipation,

$$P = 3I^2r \text{ watts} = 3 \times 14{\cdot}47^2 \times 10 \text{ W} = \underline{6281{\cdot}4 \text{ W}}.$$

(*b*) In the delta connection, the supply voltage is connected directly to the load

$$\therefore \quad I_{\text{PHASE}} = \frac{415}{16{\cdot}56} \text{ A} = 25{\cdot}06 \text{ A}.$$

$$\therefore \quad P = 3 \times 25{\cdot}06^2 \times 10 \text{ W} = 18\,840 \text{ W}.$$

In practice, the power in delta is three times as large as in star.

PART 2—Electronics (Digital) III (BTEC)

Q7 (*a*) *Obtain the minimal form of the logic function given by the truth table in Figure 3.*
(*b*) *Draw the logic circuit for* (*a*) *using only* NAND *gates.*
(*c*) *Show the circuit connections which must be made and the supply voltages if the logic circuit in* (*b*) *is to be implemented using a transistor–transistor logic* (*TTL*) *integrated circuit type 74LS00.*

A	*B*	*C*	*F*
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Figure 3

A7 (*a*) From the truth table,

$$F = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C + ABC.$$

Factorising the terms in groups of two,

$$F = \bar{A}B(\bar{C} + C) + AC(\bar{B} + B).$$

But $\bar{C} + C \equiv 1$ and $\bar{B} + B \equiv 1$.

$$\therefore \quad F = \bar{A}B + AC.$$

(*b*)

In order to convert the function of (*a*) to the NAND form, De Morgan's theorem is used.

Let $\bar{A}B = P$ and $AC = Q$.
Then

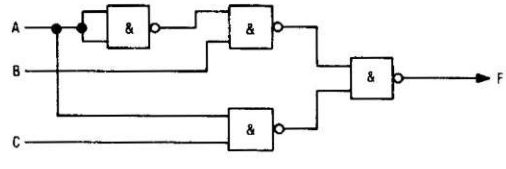
$$F = P + Q.$$

By De Morgan's theorem,

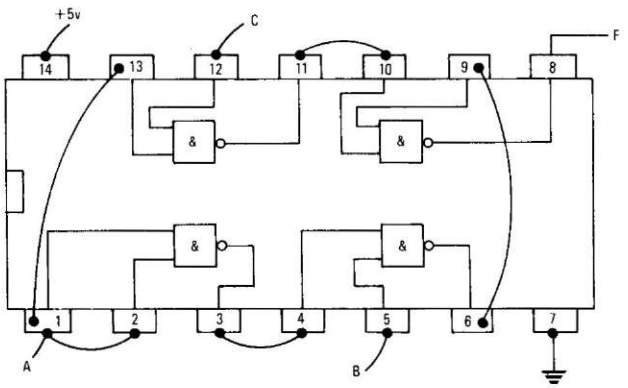
$$F = \overline{\bar{P}\bar{Q}}.$$

Resubstituting,

$$F = \overline{(\overline{\bar{A}B})(\overline{AC})}.$$



(*c*)



Q8 *The timing diagram of Figure 4(b) refers to the logic circuit of Figure 4(a) which consists of a D-bistable coupled to an S–R bistable.* Q_D *is the output from the D-bistable and Q is the output from the complete circuit.*

Redraw the timing diagram and complete the waveforms for Q_D *and Q.*

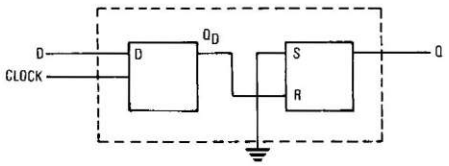


Figure 4(a)

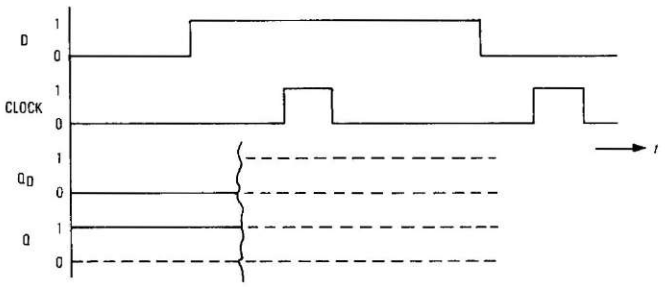
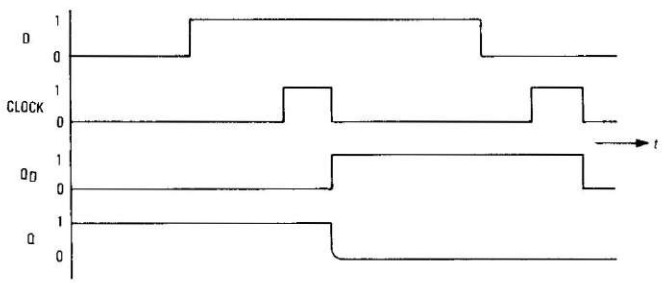


Figure 4(b)

A8



In order to avoid the ambiguous case of both S and R inputs being high, the S input of Figure 4(*a*) has been connected to chassis. This means that for the circuit shown, Q can only be reset to 0.

In the waveforms, it has been assumed that Q_D takes up the state of the D input after the clock pulse. In practice, many commercial D elements incorporate an inverter between the clock input and the bistable. When an inverter is included, Q_D takes up the state of the D input at the beginning of the clock pulse.

In practice, there will be a slight time delay between the application of the clock pulse and the output at Q. This is caused by the transmission time of the two bistables. For this reason, the Q waveform is shown slightly rounded.

When Q_D goes to 1 the S–R bistable is reset, but after this it cannot be set again unless SET and CLEAR connections are incorporated.

Q9 *The circuit of Figure 5 uses one half of a CMOS IC type 4001 whose logic levels are given as*

$$0{\cdot}7V_{DD} - V_{DD} = \text{'}1\text{'}$$

$$V_{SS} - 0{\cdot}3V_{DD} = \text{'}0\text{'}$$

(a) Show that the frequency of operation does not change as the variable resistor P is moved from A to B.

(b) Calculate the frequency of operation of the circuit.

(c) Calculate the variation of mark–space ratio as P is varied from A to B.

(d) Draw the waveform at Q when the control P is set at A. Indicate the time at which each change of state occurs, assuming that the first change of state to '1' occurs at $t = 0$.

(e) State the range of voltage at Q over which the output state may not operate another CMOS device.

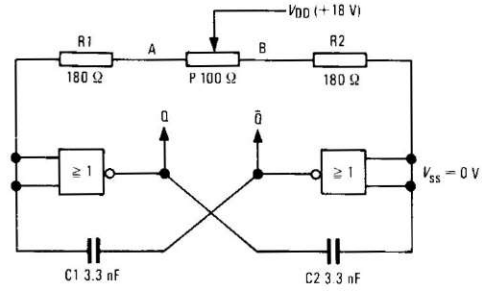


Figure 5

A9 Figure 5 shows the circuit of an astable multivibrator whose periodic time is given by

$$T = t_1 + t_2,$$

where t_1 and t_2 are the durations of the two quasi-stable states. The duration of one quasi-stable stable is given by

$$t = 0{\cdot}69CR,$$

where the value of R depends on the setting of the variable resistor P.

Let the resistance between A and the slider be x and that between the slider and B be $(P - x)$.

Then

$$t_1 = 0{\cdot}69C_1(R_1 + x).$$

$$t_2 = 0{\cdot}69C_2\{R_2 + (P - x)\}.$$

$$\therefore \quad T = 0{\cdot}69C_1(R_1 + x) + 0{\cdot}69C_2(R_2 + P - x),$$

$$= 0{\cdot}69\{C_1(R_1 + x) + C_2(R_2 + P - x)\}.$$

When $C_1 = C_2 = C$,

$$T = 0{\cdot}69C(R_1 + x + R_2 + P - x).$$

$$\therefore \quad T = 0{\cdot}69C(R_1 + R_2 + P).$$

So, when the two coupling capacitors have the same value, since x does not feature in the formula for the periodic time, the setting of P does not change the frequency.

(*b*)
$$T = 0{\cdot}69C(R_1 + R_2 + P),$$

$$= 0{\cdot}69 \times 3{\cdot}3 \times 10^{-9}(180 + 180 + 100)\ \text{s},$$

$$= 1{\cdot}047 \times 10^{-6}\ \text{s} = 1{\cdot}047\ \mu\text{s}.$$

The frequency of operation

$$f = \frac{1}{T} = \frac{1}{1{\cdot}047 \times 10^{-6}}\ \text{Hz} = \underline{955\ \text{kHz}}.$$

(*c*)

The mark–space ratio depends on the time constant in each coupling circuit, but since $C_1 = C_2$, the ratio of the resistor values can be used.

When P is set at A the ratio is,

$$R_1 : (P + R_2) = 180 : (100 + 180) = 180 : 280 = 1 : 1{\cdot}5\dot{5}.$$

When P is set at A, the time constant will be shorter than other settings so the gate Q will be off for a shorter time. This means that the output at Q is high for a shorter time. Thus, when P is set at A, the mark–space ratio at Q is 1:1·55.

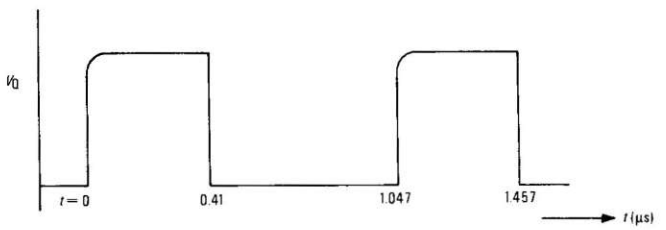
Conversely, when P is set at B the mark–space ratio at Q is 1·55:1.

(*d*) The period of one cycle is 1·047 μs. Thus the positive transition has a duration of

$$t_1 = 1{\cdot}047 \times \frac{180}{460}\ \mu\text{s} = 0{\cdot}41\ \mu\text{s}.$$

$$t_1 + t_2 = 1{\cdot}047\ \mu\text{s}.$$

$$t_1 + t_2 + t_3 = 1{\cdot}047 + 0{\cdot}41\ \mu\text{s} = 1{\cdot}457\ \mu\text{s}.$$



(*e*) The threshold voltages are given in the question so that, assuming the other CMOS devices to be connected to the same supply of 18 V:

$$0{\cdot}7 \times 18\ \text{V} = 12{\cdot}6\ \text{V} \qquad 0{\cdot}3 \times 18\ \text{V} = 5{\cdot}4\ \text{V}$$

The range of voltage between 5·4 V and 12·6 V may not successfully control another CMOS device.

Q10 *Figure 6 shows part of the circuit for an S–R bistable using discrete components and silicon transistors. TR2 is assumed to be saturated.*

(*a*) *Calculate the voltages on Q and* $\bar{Q}$.

(*b*) *Do the voltages calculated in* (*a*) *satisfy the requirements for transistor–transistor logic* (*TTL*)*? Explain your answer.*

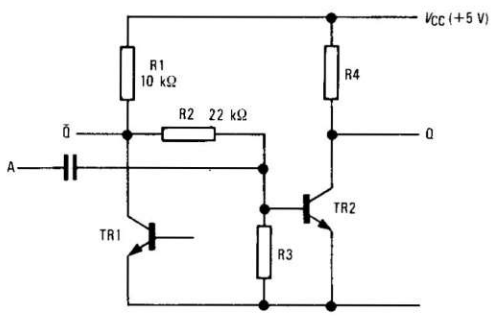


Figure 6

A10

For the silicon transistor, values of

$$V_{\text{CE,SAT}} = 0{\cdot}2\ \text{V} \qquad \text{and} \qquad V_{\text{BE,SAT}} = 0{\cdot}8\ \text{V}$$

should be used.

When TR2 is saturated, the potential difference between V_{CC} and $V_{\text{BE,SAT}}$ is voltage divided between R1 and R2. (When TR2 is saturated, TR1 is off.)

(*a*)
$$V_{\text{R1}} = (V_{\text{CC}} - V_{\text{BE,SAT}})\frac{R_1}{R_1 + R_2},$$

$$= (5 - 0{\cdot}8)\frac{10}{10 + 22}\ \text{V} = 1{\cdot}3125\ \text{V}.$$

$$V_{\bar{Q}} = V_{CC} - V_{R1}.$$

$$\therefore \quad V_{\bar{Q}} = 5 - 1{\cdot}3125\ \text{V} = \underline{3{\cdot}6875\ \text{V}}.$$

$$V_Q = V_{CE,SAT} = \underline{0{\cdot}2\ \text{V}}.$$

(*b*) The threshold voltages for TTL operation are

$$2\ \text{V} - 5\ \text{V} \equiv \text{'1'} \qquad\qquad 0\ \text{V} - 0{\cdot}8\ \text{V} \equiv \text{'0'}$$

Comparing the threshold voltages with the potentials, it is seen that $V_{\bar{Q}}$ is well above 2 V and V_Q well below 0·8 V. From this, it is noted that the voltages at $\bar{Q}$ and $\bar{Q}$ meet the requirements of TTL working.

Q11 *The series of clock pulses shown in Figure 7(b) is applied to the J–K master-slave circuit shown in Figure 7(a). During the time period t_0 to t_6, the J and K inputs are adjusted to the logic states shown in Figure 7(c).*

Reproduce the table of Figure 7(c) and complete the missing states for Q_m and Q.

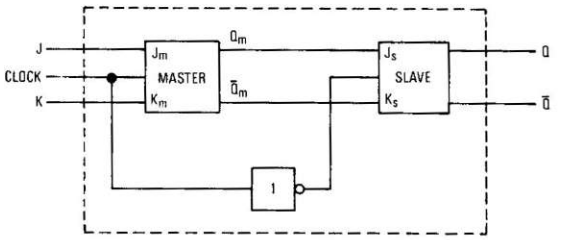


Figure 7(a)

t	*J*	*K*	Q_m	*Q*
t_0	0	0	0	0
t_1	1	0		
t_2	1	0		
t_3	1	1		
t_4	1	1		
t_5	0	1		
t_6	0	1		

Figure 7(c)

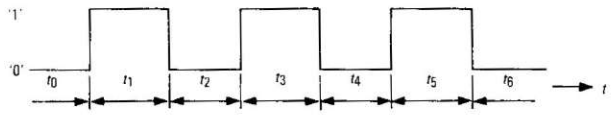


Figure 7(b)

A11

In order to determine the states for Q_m and Q, it must be realised that when the clock pulse is in the '1' state, the master bistable will be affected, during which time, the slave bistable will be held in its previous state. When the clock pulse goes to '0' the inverter enables the clock operation to the slave. The output from the slave then takes up the state dictated by Q_m and $\bar{Q}_m$, these being connected to J_S and K_S respectively.

It is best to complete the Q_m column first and then, depending on the values of Q_m and $\bar{Q}_m$, to complete the Q column.

The Q_m and Q outputs can be found by reference to the JK state change table shown below.

J	*K*	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

t	*J*	*K*	Q_m	*Q*
t_0	0	0	0	0
t_1	1	0	1	0
t_2	1	0	1	1
t_3	1	1	0	1
t_4	1	1	0	0
t_5	0	1	0	0
t_6	0	1	0	0

Q12 *Figure 8(a) shows a serial-input parallel-output shift register which uses four master-slave J–K bistables. Stage D of the shift register is considered as the most significant bit of the data held at any given time.*

(a) Draw a timing diagram to show the state of Q_A, Q_B, Q_C and Q_D during the input sequence shown in Figure 8(b). It is assumed that the shift register has been cleared of data before the start of the sequence.

(b) What is the hexadecimal value of the nibble held by the shift register at the end of the sequence?

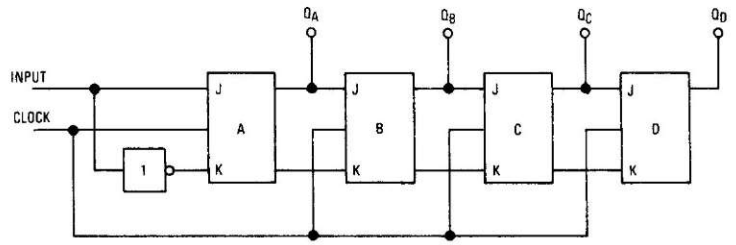


Figure 8(a)

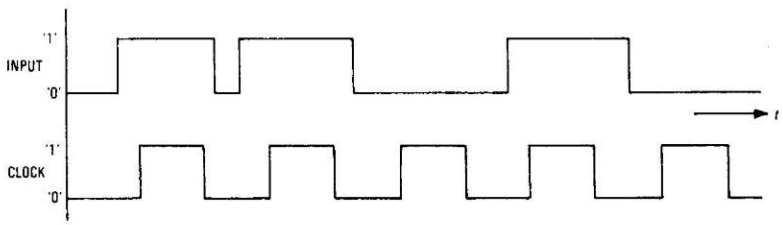


Figure 8(b)

A12

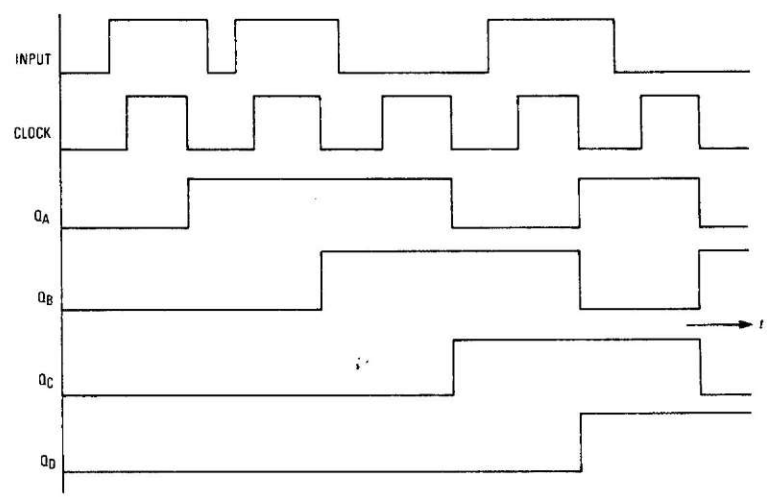
In the case of the shift register shown in Figure 8(*a*), it is possible for any given Q output to be determined by only one of two input combinations. Under no condition can the output toggle to the other state since J can never be the same value as K.

The inverter connected between J and K at the input results in a reduced state change table for the bistable.

J	K	Q_{n+1}
0	1	0
1	0	1

The use of master-slave bistables means that any given Q takes up the next state at the end of the clock pulse. The timing diagram is best drawn sequentially. First determine the waveform at Q_A after which Q_B can be found since it depends on Q_A. It will also be noted that the waveforms move diagonally across to the right as the data is shifted through the register.

(*a*)



(*b*) After 5 clock pulses, reading from the bottom of the timing diagram,

$$Q_D = 1,\ Q_C = 0,\ Q_B = 1,\ Q_A = 0.$$

The nibble held at the end of the sequence is therefore,

$$1010_2 \equiv A_H.$$

Q13 *The following components are available for use in the design of a logic circuit which will operate a large relay when a beam of light is interrupted by a passing object.*

The specification is that the current amplifier operates when its input is a '0' and that an ENABLE *signal controls the output from the* NAND *gate.*

68 kΩ resistor	*Low-power n p n transistor*
5·6 kΩ resistor	*IC current amplifier*
Photocell	*Relay*
TTL NAND *gate*	*Power supply with +5 V and +20 V.*
Diode	

(*a*) *Draw a circuit which meets the specification and uses the available components.*
(*b*) *Explain the operation of the circuit which you have drawn.*

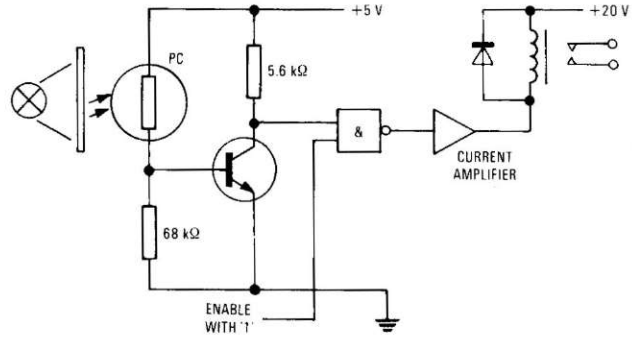
A13

It is always worthwhile when using NAND or NOR gates, to rough out a truth table. This makes it easier to see the conditions which will produce the desired result.

A	*B*	*AB*	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Inspection of the truth table shows that the only condition which gives a change of state at the output is when A and B change from one '1' to two '1's. This means that in order to meet the specification, the NAND gate must be enabled by a '1'. In addition, the other input to the NAND gate must also go to '1' when the beam of light is interrupted.

(*a*)



(*b*) When the beam of light strikes the photocell, its resistance falls. The voltage division between PC and the 68 kΩ resistor is now such that the transistor is forward biased and collector current flows. The volt drop across the collector load is now sufficient to make the input to the NAND gate a '0'. The output from the NAND gate must now be '1' irrespective of the state of the enable line and therefore no current flows through the relay.

When the beam of light is interrupted, the resistance of the photocell goes high with the result that the transistor is cut off. No current flows through the 5·6 kΩ resistor to the collector so that the input to the NAND gate is a '1'. If simultaneously the ENABLE line is '1', the NAND gate sees two '1's at its input, and outputs a '0' to the current amplifier. Current now flows through the relay and it is energised.

The diode is connected across the relay such that it does not conduct when current is passing through the relay to the current amplifier (the cathode is connected to +20 V). When the current amplifier is switched off, the stored magnetic energy in the relay produces a large EMF of opposite polarity which drives a current through the diode. This rapidly dissipates the stored energy. In the absence of the diode, the induced EMF produced on switch-off could be sufficient to cause electrical breakdown of the amplifier.